RESPONSE under 37 C.F.R. § 1.111
U.S. Appln. No. 10/788,718

IN THE DRAWINGS:

The appended drawing sheets include an annotated version showing changes to Figs. 3 and 4 (sheet 3). This sheet amends original Figs. 3 and 4 at 3 instances changing the word "LINE" to "LOOP" as requested in the Office Action dated March 23, 2006. Also included are Replacement Sheets 1-4 (replacement sheets 1, 2 and 4 do not include any changes) are provided to replace the original informal drawings with formal drawings.

ATTACHMENT: Replacement drawing sheets 1-4
Annotated Figs. 3 and 4 (sheet 3) showing changes

REMARKS:

Claims 1-23 are pending in the application and stand rejected. Reconsideration and allowance of all pending claims are respectfully requested in view of the following remarks.

OBJECTIONS.

Specification

The Examiner objects to the specification and requests that Applicant provide a SUMMARY OF THE INVENTION section in the present application. However, Applicant respectfully submits that neither the MPEP nor 37 C.F.R. §1.77(b)(1) require the presence of a "Summary of the Invention." They merely indicate where in the application the "Summary of the Invention" should be placed if it is included. 37 C.F.R. §1.73 only states that a "Summary of the Invention" should or may be included; it does not state "must" or "shall" (See 37 C.F.R. § 1.71 language). Accordingly, Applicant has elected not to include a "Summary of the Invention" as within the discretion of the Applicant. Furthermore, virtually none of the thousands of patent applications filed each year on behalf of the current assignee include summaries, including the parent patent to this application (US 6,757,817), because there is no rule, regulation or precedent which has ever required that a Summary be present in a patent application. Notwithstanding, if the Examiner is able to cite any regulatory or legal precedent which demonstrates that an Applicant can be denied a patent solely on the basis of objection for lacking a Summary of the Invention section, Applicant is willing to reconsider its position. Absent such showing, objection to the specification has no proper basis and reconsideration of this objection is respectfully requested.

In contrast to the mere suggestion by the CFR that a Summary of Invention should be included, Applicant has amended the specification to include the required Cross-reference to Related Applications section as specified under 37 C.F.R. § 1.78(a)(2).

Drawings

Figs. 3 and 4 of the drawings are objected to based on alleged inconsistencies between the specification and the depicted embodiments. In response to this objection, Applicant amends the drawings as shown above and provides formal copies for all drawing sheets, including the amendments to Figs. 3 and 4, in Appendix A which follows.

CLAIM REJECTIONS.

Double Patenting

Claims 1-23 are rejected under the judicially created doctrine of obviousness-type double patenting. Applicant disagrees with the Office Action premise. For example, original claims 4, 5, 8 and 11-17 have been indicated in the record of this application AND the issued parent file history as having patentable subject matter while independent claims 1 and 9 have thus far been alleged to be unpatentable. Therefore it follows that claims 4, 5, 8 and 11-17 are considered by the Office to be separately patentable over Applicant's independent claims 1 and 9 and consequently, by the Office's own interpretation, these claims cannot be an obvious variants to these claims. While claims 4, 5, 8 and 11-17 may be obviousness-type variants in view of the claims in issued U.S. 6,757,817, all of Applicant's claims 1-23 cannot be. Notwithstanding, to advance the prosecution of this case, Applicant submits herewith, a terminal disclaimer to obviate this rejection. In light thereof, reconsideration and withdrawal of this rejection are respectfully requested.

35 U.S.C. § 103(a)

1.) Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. 5,353,426 to Patel et al. (hereinafter "Patel") in view of U.S. 6,085,315 to Fleck et al. (hereinafter "Fleck"). Applicant respectfully traverses this rejection for the following reasons.

It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary sill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

The Office Action alleges that Patel discloses all of the limitations of Applicant's claim 1 except that "Patel did not specifically teach his buffer was a loop buffer as claimed" and relies on Fleck's loop cache buffer 3 to make up for this deficiency. The Office Action alleges: "[i]t would have been obvious to one of ordinary skill in the art to use Fleck in Patel for using the loop buffer for determining if at least a portion of the instruction was stored in a buffer as claimed because the use of Fleck's loop buffer could provide the capability to reduce the number of times a given request made frequently to the cache array of Patel, thereby minimizing the R/W cycle, and it could be achieved by defining the I/O ports of the loop buffer of Fleck into Patel's configuration, and because Patel already taught the use of a buffer [cache miss buffer] in addition to a cache to reduce the wait time (citation omitted), although the buffer was not used as loop buffer, one of ordinary skill in the art should be able to recognize Fleck's loop buffer which was used in addition to a cache subsystem (citation omitted) for storing instructions frequently used to minimize memory access time (citation omitted) could have provided a solution to Patel's cache array, and, and doing so provided the motivation." (3/26/06 Office Action pgs. 8-9).

To the extent that Applicant is able to comprehend the reasoning set forth in the Office Action for combining the cited references, Applicant respectfully disagrees.

Patel

Patel discloses conventional cache architecture of a type similar to that discussed in Applicant's Background section. (Specification pg. 1). Namely Patel discloses a cache array for storing pre-fetch instructions and/or data that a processor is likely to request in upcoming instruction cycles. (Col. 1, ll. 14-22). However, Patel discloses an approach to fetching data from cache memory which allows read and write operations to be performed in the same clock cycle to further reduce CPU idle time. (Col. 2, ll. 52-55). To this end, Patel proposes the use of a cache tag and comparator unit 46 or 52 which includes a tag array 64 (Fig. 3), a cache miss buffer 66 and control logic 68 which are used to describe which memory block frames are currently cached and where they are cached in the separate cache array 50. (Col. 3, ll. 18-26 and col. 7, ll. 44-49).

Therefore, by no stretch of the imagination does Patel disclose or suggest *determining if at least a portion of the instruction* (for execution) *is stored in* any type of buffer whatsoever, and certainly not cache miss buffer 66. Applicant respectfully directs the Examiner to Patel col. 8, ll. 48-55 for proper understanding of what is stored in cache miss buffer 66. That is, there are no instructions or data for execution to be stored in Patel cache miss buffer 66, rather buffer 66 is used to store descriptive information to "describe the current state of a cache fill." (Col. 8, ll. 54-55). Accordingly and respectfully, the entire premises on which Office Action bases its rejections appear to be fundamentally flawed.

While Fleck does disclose a loop cache buffer 3, there is simply no motivation or reason why the skilled artisan would replace Patel's cache miss buffer 66 with Fleck's loop cache buffer 3. This is primarily due to that fact that Patel's cache miss buffer merely stores descriptive information regarding a fill state of a cache whereas Fleck's loop cache is actually used as a cache (i.e., to store temporary data or instructions for execution by a processor). Because the proposed combination of Patel and Fleck appears incompatible, there is no proper motivation for

combining the references as alleged in the Office Action. Accordingly, *prima facie* obviousness has not been established.

Moreover, even assuming it would be proper to modify Patel with the loop cache buffer of Fleck (*arguendo*) Applicant respectfully submits the resultant combination would still fail to teach or suggest the limitations recited in Applicant's claims 1-3. Namely, even if Patel cache miss buffer 66 were modified to be a loop cache buffer 3 of Fleck, there is simply no teaching or suggestion by the cited references that both a loop buffer AND a cache would be checked *to determine if at least a portion of the instruction* (for execution) *is stored in* both *a loop buffer* and a *cache*. Since Patel and Fleck, taken alone or in any combination fail to teach or suggest at least these recitations, *prima facie* obviousness is not established. For the foregoing reasons, Applicant respectfully requests the Examiner to reconsider and withdraw the §103 rejection of claims 1-3.

2.) Claims 6-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel in view of Fleck in further view of U.S. 6,154,814 to Uesugi. Applicant respectfully traverses this rejection for the reasons that follow. The Office Action cites Uesugi to disclose *a tag register* in Applicant's claim 3, which is admittedly not disclosed or suggested by the combination of Patel and Fleck. Applicant respectfully submit that this rejection is unfounded for at least the reasons previously discussed; namely that there is no proper motivation for combining Patel and Fleck as proposed and even when combined, the features of Applicant's claim 1 (from which claims 6-7 depend) are not disclosed or suggested. Since Uesugi fails to remedy the deficiencies previously noted with regard to the combination of Patel and Fleck, *prima facie* obviousness has not been established and Applicant respectfully requests reconsideration and withdrawal of this §103 rejection as well.

3.) Claims 9-10, 18-19 and 20-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. 5,958,040 to Jouppi in view of U.S. 6,535,583 to Bobick et al. (hereinafter "Bobick"). Applicant respectfully traverses this rejection for the following reasons.

The Office Action expressly admits that Jouppi does not teach a loop buffer as recited in Applicant's independent claim 9. The Office Action relies on Bobick to make up for this deficiency alleging it would have been obvious to one of ordinary skill in the art to use the loop buffer 140 of Bobick in Jouppi to "provide the processing ability of Jouppi to accept a predetermined set of repeatedly executed instructions at a given request and at a given set of address space, ...

However, Applicant respectfully points out, without acquiescing to the properness of the alleged motivation for combining these references, that even modifying the teachings of Jouppi with those of Bobick as proposed, Applicant's claim 9 recitation of *enabling a portion of the memory array corresponding to the loop buffer* is not disclosed or suggested. This is due to the fact that Bobick discloses only a use for loop buffer 140 for storing codes representing a loop counter (col. 10, ll. 17-18) which does not appear to have anything to do with *enabling a portion of the memory array corresponding to the loop buffer*. Since Jouppi and Bobick, taken alone or in any combination, fail to disclose or suggest at least these features of Applicant's independent claim 9, *prima facie* obviousness is not established with respect to claim 9 or claims 10 and 18-19 which depend from claim 9.

In respect to Applicant's independent claim 20 which recites:
an apparatus having an integrated circuit, the integrated circuit comprising: a memory array adapted to provide a loop buffer and a cache, neither Jouppi or Bobick disclose an integrated circuit including these elements and thus *prima facie* cannot be established with respect to claim 20 or any claim which depends there from. Lastly, Applicant disputes the Office Action's alleged motivation to replace Jouppi stream buffer 120 with Bobick's loop buffer 140. Because stream buffer 120 merely queues cache data or instructions between Instruction cache 118 and/or Data cache 116 to CPU 112, there would appear to be no purpose for using the loop buffer of

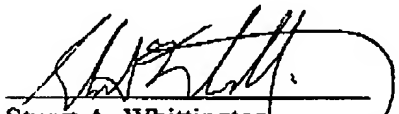
Bobick which merely stores a loop count (as opposed to cache data or instructions) and in fact, replacing Jouppi stream buffers 120 with the loop buffer 140 of Bobick would appear to render the primary reference (Jouppi) unsuitable for its intended purpose.

For all the foregoing reasons, Applicant respectfully submits *prima facie* obviousness has not been established with respect to Applicant's claims 9-10, 19 and 20-23 and respectfully requests the Examiner to reconsider and withdraw the §103 rejection based on Jouppi and Bobick.

CONCLUSION.

In view of the above, reconsideration and allowance of this application is now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee or deficiency thereof, except for the Issue Fee, is to be charged to **Deposit Account # 50-0221.**

Respectfully submitted,



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